Development of Portable Cardiograph Using Novel Front-End Solutions

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***Abstract*—In this paper, we propose a structure of a portable cardiograph. Contents and functions of all blocks are overviewed. We describe two main structures of portable cardiographs, prepare a comparative table of characteristics for different analog front-ends. All individual features of the chips are listed as well. We register a test signal and try to improve its quality by means of digital filtration, taking the signal gained from certified Biopack equipment as a reference. We calculate device power consumption to compute required battery volume. Finally, energy efficient preprocessing algorithm is proposed.**

I. Introduction

The correct functioning of the persons cardiovascular system largely determines the quality level of his life. It supports the work of the necessary mechanisms of the body: nutrition, respiration, removal of metabolic products and others. However, sometimes problems in the work of the cardiovascular system are not expressed in sufficiently obvious symptoms for a person to consider it necessary to visit a medical institution for examination. For example, such a violation of the rhythm of the heart as extrasystole can be found throughout 60-70% of the world's population and in most cases it is the result of stress on the human nervous system (smoking, stress, alcohol, lack of sleep, etc.).

In the case of neurogenic nature of the disease, we can talk about low risk to human life and treatment is reduced to the elimination of provocative factors, for example, normalization of the day and night cycle. On the other hand, if the extrasystole is caused by pathological processes in the heart at the physical level, the development of this disease through several stages will inevitably lead to a heart attack if left untreated.

Microelectronics development and increasing popularity of portable devices have led to a proliferation of portable cardiographs, although their accuracy is still questionable [1], [2]. We are talking about devices for medical applications (i.e. ambulance cardiographs or Holter monitors) and personal devices for monitoring of ECG by the patient himself.

Such devises have to fuse features of a portable device with such of an appliance for biomedical measurements:

- Low power consumption
- High accuracy
- High reliability
- Small size

All of the requirements above can only be satisfied by using the latest and most efficient circuitry. In this paper, we decided to make a comparison of front-end circuits from different leading manufacturers and propose a structure of a portable cardiograph, based on them.

II. Structure of a Device

Let's take a look at the proposed structure (Fig. 1).

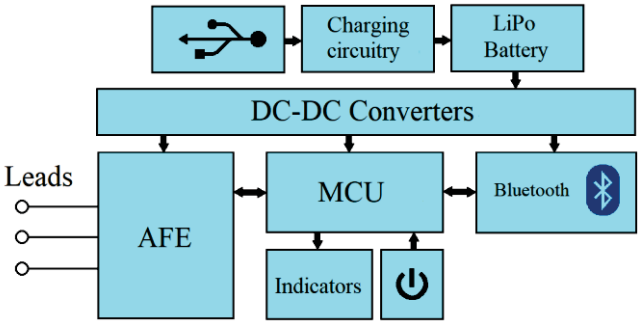

Fig. 1. Structural scheme of a portable cardiograph

A. Front-end circuitry

The most important part of the cardiograph is its front-end, which is responsible for recording biopotentials from the subject and converting them into a digital code for future processing. Besides common requirements such as high accuracy and reliability, low power consumption and high common mode rejection ration are necessities. Additional features, specific for cardiograph front-ends such as leads-off detection are always nice to have.

A strong analysis of modern analog front-ends (ADS1292R, MAX30003, ADAS1000 and AD8232) for portable cardiographs is provided in section III.

B. MCU

The tasks for the microcontroller are to control and synchronize the operation of the device units, preprocess the recorded signal "on board" and transfer data to another computing device using Bluetooth module. Also, the microcontroller monitors the battery charge and provides information to the user through the indication system.

Taking rather small power amount into account, deep data processing using MCU is unavailable. That's why power-efficient solutions with a variety of power-saving modes of operation are prioritized. For example, an Atmel ATmega328P microprocessor is capable of running using ultra low supply voltage of 1.8 V with current consumption of only 2 mA.

C. Communication

Communication block consists of two parts: a communication interface between device and a user and a data transfer interface. The first one is simple. A button and a RGB LED are capable enough to provide simple power switching and device's state indication.

As for data transferring, the most promising "second stage" device is a user smartphone. There are three main methods for data transferring available: using a USB cable, Bluetooth or WiFi. The first one requires direct connection between two devices, which renders cardiograph portability useless as soon as smartphone needs charging. Despite great range and throughput, Wi-Fi consumes too much power so it is unusable in low-power applications.

Bluetooth doesn't have these drawbacks and meets all of the portable device demands. Texas Instruments provides CC2541, a low energy Bluetooth system-on-chip, which is perfect for our application, as it can operate at 3.3 V power supply. For further reduction in data transferring and power consumption one may consider using compression methods [3].

D. Power circuitry

A rechargeable LiPo battery (3.7V nominal) provides enough power for a device operation. For safety reasons, a control circuitry is used, which handles charging voltage and current as well as protects battery from over discharge. A widespread USB connector is recommended for charger connection. The battery voltage is converted via a set of DC-DC converters based on linear stabilizers, forming all necessary voltages for device operation.

All circuits proposed above require either a 3.3 V supply voltage, or 1.8 V. We suggest using a boosting converter based on the NCP1402 (ON Semiconductor) chip for acquiring 5 V, which then are stabilized to 3.3 V and 1.8 V by ADP150 and ADP151 (Analog Devices) linear stabilizer respectively.

Bq24202 circuit from Texas Instruments is a popular solution as a charge management controller.

III. Front-end circuitry

A. Structure overview

Typically, such devices are built using discrete components following common structure (Fig. 2) [4], [5]. A typical ADC full-scale voltage is approximately 2.5 V, which means a gain of 500 (assuming a 5-mV input signal). The total gain is spread between the instrumentation amplifier (INA) and an additional gain amplifier. Gain should be added to the INA in such a way that the electrode dc offset does not saturate the INA. Before any further amplification, the dc component must be removed. That is why a high-pass filter (HPF) with a stop frequency of 0.05 Hz is added. Once the dc component is removed, the signal is gained up again with another amplifier. It should be noted that the amplifiers used for these gain stages must be very low noise, so that they do not dominate the noise of the system. Speaking of portable devices, these amplifiers should be low power as well. This combination increases the cost of the precision amps required by the system.

The gain stage is followed by an antialiasing filter. Typically, a fourth order or higher active low-pass filter (LPF) is used. Finally, a multiplexer block (mux) feeds signals into the ADC.

It is obvious, that all signal processing, including filtering and gain, is analog. It gradually limits flexibility of the system.

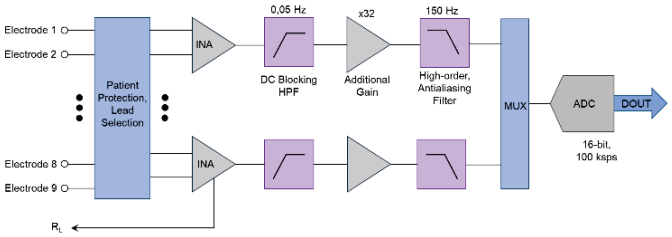

Fig. 2. Structure of a standard SAR-based cardiograph

Since digital signal processing is relatively lower cost and provides a great deal of flexibility, it is beneficial to move the signal processing to the digital domain. On the Fig. 3 the same ECG analog front-end (AFE) with a delta-sigma ADC implemented is shown. Traditionally, delta-sigma ADC speeds were limited to sampling rates of several kilohertz, but technology advancements have led to increasing them to hundreds of kHz, while perfect DC and AC characteristics are intact [6].

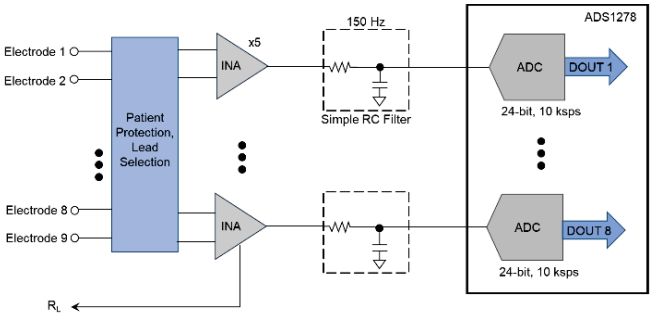

Fig. 3. Structure of a Sigma-Delta ADC based cardiograph

In the Fig. 2 the structure of ADS1258 used for the ECG front-end is shown. By comparing Fig. 2 and Fig. 3, it can be seen that there is a significant reduction in hardware, which leads to both lower cost and lower power. Most of the blocks (including the high-pass filter, dc blocking filter, gain stage, and a steep, active low-pass filter) are eliminated. In addition to offering the advantage of higher resolution, the delta-sigma ADCs has significantly lower antialiasing requirements. The complicated active antialiasing filters, which could require several amplifiers to implement, can be replaced by a simple, single-pole RC filter [7].

TABLE I. COMPARISON OF THE MAIN CHARACTERISTICS OF ANALYZED FRONT-ENDS

	ADS1292R	**ADAS1000**	**MAX30003**	**AD8232**
Manufacturer	Texas Instruments	Analog Devices	Maxim Integrated	Analog Devices
Channel amount	2	**5**	1	1
CMRR	**120 dB**	105 dB	100 dB	80 dB
Power consumption	335 uW/channel	Up to 21 mW	**240 uW/channel**	170uA
Power source	Analog: 2.7 .. 5.25V Digital: 1.7 .. 3.6V	3.15 .. 5.5V	1.1 .. 2V	2 .. 3.5V
Amplification	1, 2, 3, 4, 6, 8 or 12	1.4, 2.1, 2.8 or 4.2	**20 to 160**	100
ADC resolution	**24**	Up to 19	18	External ADC
Sampling frequency	125 .. 8000 Hz	2, 16, 128 kHz	125 to 512 Hz	External ADC
Signal-to-Noise ratio	**107 дБ**	100 дБ	77.2 (Amp = 20) 96.5 (Amp = 160)	External ADC
Right leg drive	**Yes**	**Yes**	No	**Yes**
Interface	SPI	SPI	SPI	Analog out
Pricing*	8.24$	31.69$	5.46$	**3.19$**

*Octopart pricing (https://octopart.com)

The dc blocking filter is eliminated as well, because the inherent noise of the ADC is significantly lower than the previous solution and total gain value can be much lower. This way, the dc information is not lost. Digital filter implementation also allows the use of adaptive dc removal filters for overall faster response and better rejection performance.

B. Feature Comparison

The analysis of the market showed that all main companies have their own interface chips for biological potentials registration. Several features are common throughout all analyzed chips:

- Electrostatic discharge (ESD) protection
- Electromagnetic filtering
- Leads-off detection
- Calibration voltages for built-in self-test
- High input impedance
- Low noise, high linearity
- High common mode rejection ratio (CMRR)
- Programmable gain INA
- High-resolution ADC
- Small package (without external elements)
- Low power consumption
- Integrated Respiration Impedance Measurement

Most important electrical characteristics of the compared microchips are shown in the Table I. The source of information is the official datasheets. The best values in categories are marked as bold.

Texas Instruments has a family of front-end circuits with different channels number. For our work, we have chosen ADS1292R. All chips have some important features:

- Built-In Oscillator
- Digital Pace Detection Capability;
- Flexibility for pace detection by using either software or external hardware;
- The option of connecting external hardware to the output of the PGA to detect the presence of the pulse.

MAX30003 chip from Maxim Integrated has the lowest energy consumption and provides a variety of features for additional power economy.

- Built-In Heart Rate Detection which eliminates the need to Run HR Algorithm on the µController;
- Robust R-R Detection in High Motion Environment at Extremely Low Power;
- Various low-pass and high-pass filter programmable options;
- The differential DC rejection corner frequency is set by an external capacitor (CHPF). Recommended options are for the cutoff frequency of 4.4Hz, 0.4Hz, and 0.04Hz;
- Decimation filter consisting of a Cascaded Integrator Comb (CIC) followed by a programmable FIR filter to implement HPF and LPF selections. The high-pass filter options include a 1st-order IIR Butterworth filter with a 0.4Hz corner frequency along with a pass-through setting for DC coupling;
- Hardware to detect R-R intervals using an adaptation of the Pan-Tompkins QRS detection algorithm. The timing resolution of the R-R interval is approximately 8ms.
- External 32.768 kHz Clock that Controls the Sampling of the Internal Sigma-Delta ADC and Decimator.

Analog Devices in their circuit ADAS1000, in contrast with other manufacturers, using 14-bit ADC with a sampling frequency of 2.048 MHz. After processing of x1024 oversampled signal effective resolution is comparable with other competitors.

- Internal pace detection algorithm on 3 leads Support for the user's own pace;

- Scalable noise vs. power control, power/noise scaling architecture where the noise can be reduced at the expense of increasing power consumption;
- Signal acquisition channels may be shut down to save power;
- Data rates can be reduced to save power;
- The shield drive amplifier is a unity-gain amplifier. Its purpose is to drive the shield of the ECG cables;
- Four selectable low-pass filter corners are available at the 2 kHz data rate;

Another chip from Analog Devices, AD8232, is a fully integrated analog chip for biopotential measurements. The main feature is a unique input stage architecture: transconjuctival INA made on two highly complemental current amplifiers, which provides high CMRR (up to 80 dB). The clear signal can be gained without any additional notching filters implemented. Built-it integrator, working as 2nd order HPF, eliminates dc offset drift caused by bad leads contact. Additional operational amplifier allows implementation of in-built LPF and provides required gain value.

C. *Performance test*

For the experimental part of the work, AD8232 prototype board was designed and manufactured. MAX30003 official board was bought. Test signal was generated by Fluke ProSim 4. This device is capable of simulating normal sinus rhythm of vide rate range, as well as all specter of common arrhythmias. For the experiment Fluke is set on normal sinus rhythm, 60 beats per minute. Electrodes were connected to right and left arms (I lead), as well as to right leg for additional noise rejection.

As a reference cardiograph certified Biopack MP36 data acquisition unit was used. It is a high quality modular system for measurement of most commonly used biopotentials (i.e. ECG, EEG, breath characteristics, AD, etc.), meant to be used in teaching and science. For ECG recording 24-bit ADC is used. Other characteristics are: SNR greater than 89 dB, CMRR greater than 110dB, in-built notching 50Hz digital filter. Sampling frequencies are 500 Hz for Biopack and AD8232, 512Hz for MAX 30003. All filters of AD8232 and MAX 30003 were turned off. Each circuit was used for acquiring data of 40 to 50 seconds.

All signal processing and analysis is made in MatLab software. For comparison of the "raw" signals, one of the cardiac cycles was cut off the signals, the trends were removed, signals were normalized and synchronized (Fig. 4). Compared to the reference signal, which does not have even a bit of noise after digital filtration, the quality of the other two may not feel like very good, although it's obvious, that carrier signal is definitely ECG.

That is where we need to recall the structure of the cardiograph, built on a base of front-end circuit. Gained signal is meant to be digitally filtered before any further applications.

Let's take a look at that noise using Fourier transformation. A test signal is periodic, so transformation error is minimal. Looking at the results (Fig. 5), we see a frequency of the local mains power supply interference – 50Hz. Even high CMRR's of interface chips cannot reject that noise completely.

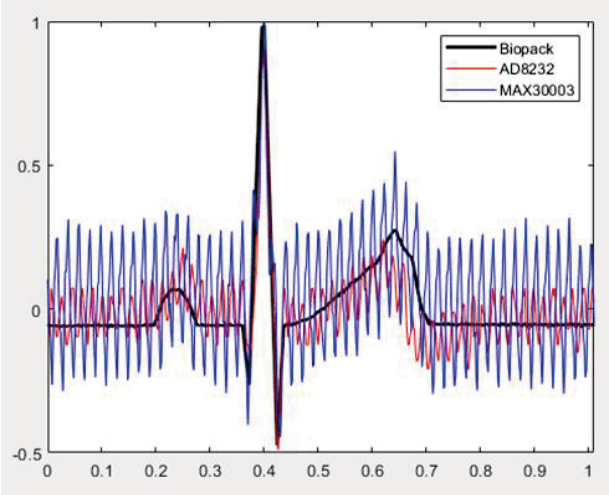

Fig. 4. "RAW" signals from different sources

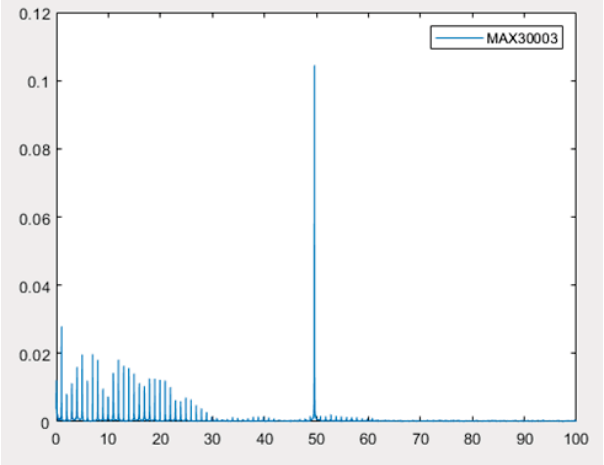

Fig. 5. Fourier transformation of MAX3003 signal

The last step of our experiment is try to remove noise from the front-end circuit signal. We decided to work on signal gained from MAX3003, as it has stronger noise, then AD8232's signal. First of all, 50Hz must be removed. Digital notching filter with the infinite impulse response (IIR), set to notching frequency of 50Hz was created and applied to the signal.

After that, we decided to apply a low-pass filter to reject everything above 150Hz (it's basically similar to filtration described in Fig. 2). Finally, the resulting signal has satisfying quality. It is still not as good as the reference one and its shape is a little bit distorted by filters, but overall performance is extremely good for such inexpensive solution (approximately 6$ for MAX30003 chip without external components).

D. *AFE conclusions*

The experiment showed high potential of front-end circuits for designing portable cardiographs on their base. After simple filtration using notching and low-pass filters, the quality of the signal has become comparable with that gained from Biopack system. Each of analyzed circuits has its own benefits and downsides.

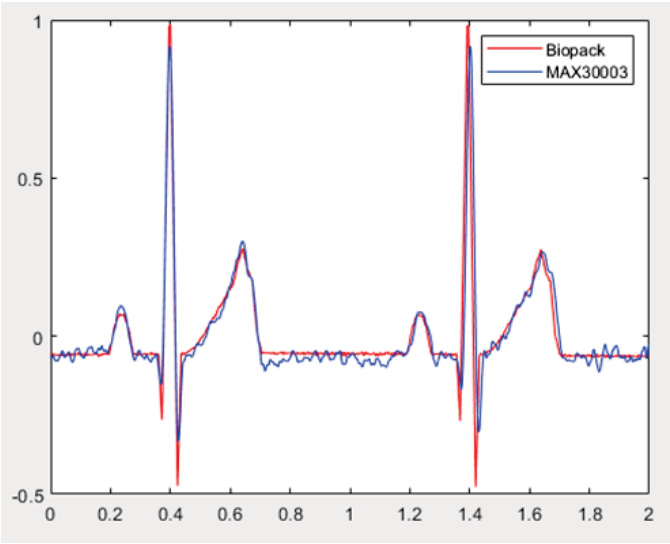

Fig. 6. Digitally filtered MAX30003 signal.

ADAS1000 has the biggest number of channels (it worth noting that ADS129x family has up to 8 channels at a cost of lower power efficiency and higher pricing compared to ADS1292R). Also, because of oversampling used to increase ADC resolution, it's possible to set sampling frequency to higher values – up to 128kHz, reducing effective accuracy. ADS129x family seems to be the most accurate of compared chips: the highest values of CMRR, signal-to-noise ratio (SNR) and 24-bit ADC. Also it is provided with internal oscillator, eliminating the need in installing one by board developers.

MAX30003 is the most power efficient chip, which came at a cost of lower CMRR, SNR, max sampling frequency and ADC resolution. Although, hardware to detect R-R intervals using an adaptation of the Pan-Tompkins QRS detection algorithm is a very interesting and unique feature, saving additional power on signal processing. Additionally, it has the lowest price within circuits with built-in ADCs.

Finally, AD8232 kind of further development of INA, provided with its own power stabilizers, right leg drive, leads-off detection, EMI protection and other useful features. Either of these AFEs can be a core of a portable cardiograph, depending on the main focus of the device.

IV. Power Consumption

The main feature that distinguishes a portable device from a stationary one is the power supply from the battery. To achieve the required operational duration, it is necessary to minimize power consumption of the device and, taking achieved level of consumption into account, correctly choose the volume of the battery. The current consumption of each of the blocks considered earlier are presented in Table II.

TABLE II. Power Consumption

Block name	Consumption, mA
AFE	< 0,5
MCU max	< 2
MCU idle	0,4
Bluetooth transmission	< 20
Bluetooth idle	< 0,3

There are several operating modes to consider power consumption:

- Device is idle, ECG is not recorded, consumed current 1 mA;
- ECG recording with on board processing (no Bluetooth data transferring), consumed current 3 mA;
- ECG recording with serialized Bluetooth data transferring, consumed current < 10 mA;
- ECG recording with constant Bluetooth data transferring, consumed current 23 mA;

Low power Bluetooth is capable of operating at 115200 baud-rate which provides extra throughput of the channel. That's why it is possible to serialize data transferring, drastically reducing power consumption.

If the target operating duration is 24 hours, taking power converters performance into account, 300 mAh battery should be sufficient power supply.

Obviously, the biggest unit in terms of physical size is this battery. The typical size for 300mA volume is 4 mm height, 25 mm width and 35mm length. Final device dimensions should be rather close to these.

V. Rhythmogram Analysis

One of the main requirements for portable devices is their long battery life. It requires high efficiency hardware and software, because a high-performance microcontroller during computation will consume too much energy (see Table II). The most accurate modern algorithms [8] are too heavy to be implemented in a wearable device. In this regard, we propose a processing algorithm that analyzes the time parameters of the ECG signal, which does not require a large amount of computing power or a large amount of RAM from the MC. In case of using MAX30003 AFE as a registering system in-build hardware R-teeth detection additionaly reduces the amount of work on signal processing. In fact, when processing "on board" the ECG signal itself will not participate in it.

The proposed algorithm is able to determine such arrhythmias as loss of ventricular complexes and various types of extrasystoles, as well as to evaluate their main time parameters, which is extremely important for assessing the risk of violations for human health:

- frequency;
- density (one, two or more extrasystole in a row);
- regularity;

Structural scheme of the algorithm is shown on Fig. 7.

At the beginning of the device operation, the algorithm analyzes the RR intervals and assuming that most of the patient's heart contractions belong to the normal rhythm, determines the average duration of the normal RR interval (T0). After the initial setup, the duration of each next registered RR interval (Ti) is subjected to interval estimation. If Ti is greater than 0.9*T0 and less than 1.1*T0, the incoming interval is considered normal and the average duration of the normal RR interval is adjusted according to the new value. This will allow to respond to natural changes in heart rate.

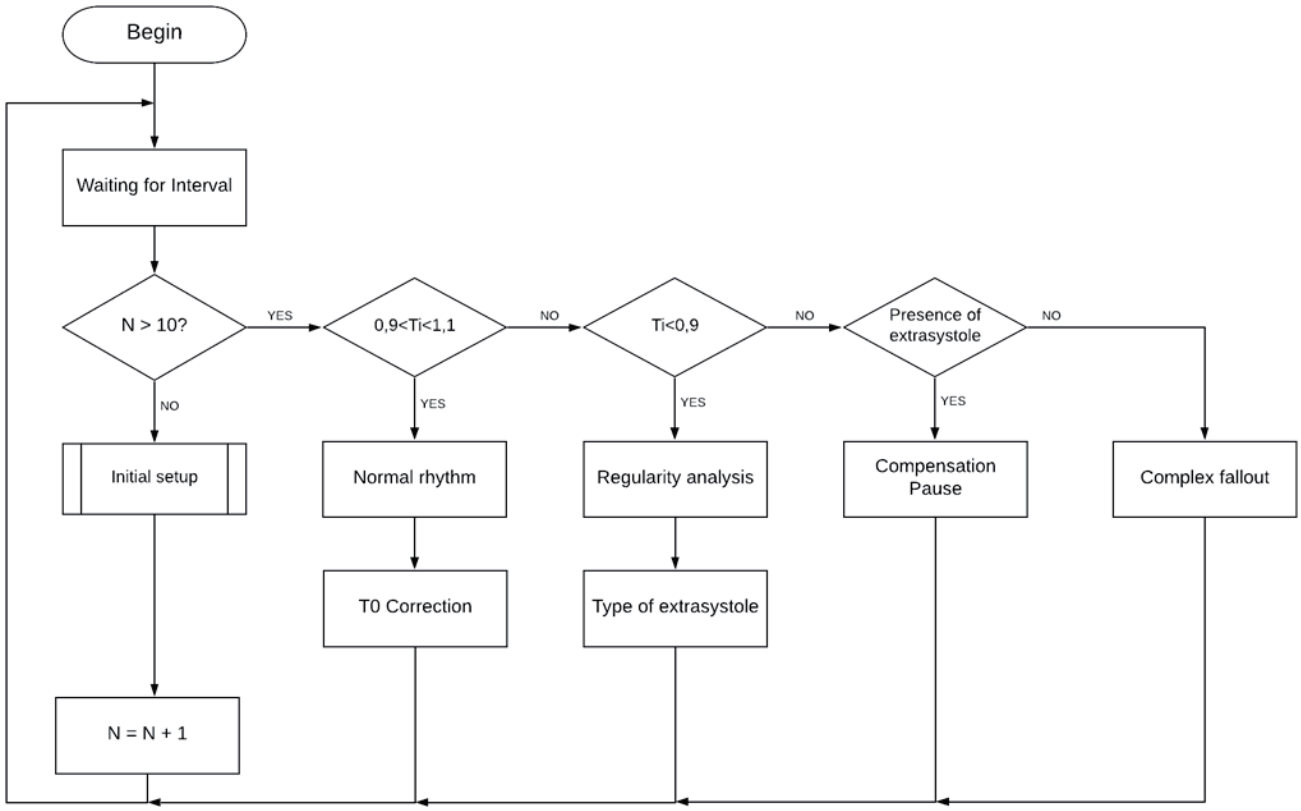

Fig. 7. Structural scheme of “on board” processing

If the next RR interval does not fall within the range of "normal" values, the interval evaluation classifies it as an episode of extrasystole in the case of Ti less than 0.9*T0 or as a ventricular complex prolapse in other cases. The memory of the MC stores the previous 50 recognized intervals, which allows us to conclude that the regularity of the violation (extrasystole through one/two/three normal complexes). Violations are also counted for each hour of observation.

VI. Conclusion

In this paper a typical structural scheme of a portable cardiograph was overviewed, its blocks and their purpose were described. Integrated circuits for each of the blocks were proposed with a main focus on minimizing power consumption thus increasing the autonomy of the device.

Additional attention was paid to the analysis of analog front-ends, their common features and differences between chips from different manufactures. The main electrical characteristics were summarized in a Table II. Real performance of the chips was measured during experiment with test generator and digital filtering. Conclusions about the possible use of each of the ICs were made.

Expected power consumption of such device was calculated. It helps to choose a correct battery volume for providing sufficient operating duration.

Finally, power efficient algorithm, utilizing AFEs features, was proposed.

Acknowledgment

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