SRAM Design Issues and Effective Panacea at Different CMOS Technology Nodes

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***Abstract*—In this paper authors analyze comprehensively the 6T SRAM cell. Solutions for different 6T design issues are also reported. While covering these solutions authors have accounted for different technology nodes. SNM and leakage power optimizations are focused on with different SRAAM topologies. 7T SRAM reported to have better RSNM and WSNM as compared to other architectures. The area overhead of 0.4µm^2 is justifiable with enhanced enhanced stability. Simultaneously 5T SRAM cell reduces the leakage power to be about 94% along with area benefits.**

I. INTRODUCTION

Static Random Access Memory (SRAM) is one of the critical elements in almost all applications of microelectronics, SOC, and VLSI chips. The benefits of high-speed operation and low power consumptions they are widely used in cache memories in microprocessors specially with multi-core architectures [1]. Rigorous efforts are put to minimize the area requirements. The Laboratory of Electronics and Information Technologies (LETI) researchers provided a breakthrough path for reducing memory bottleneck in the complex SoC's, in which up to 90% of the SoC area might be taken up by SRAM. The complexity and size of the of integrated circuits are increasing rapidly powered by transistor scaling benefits [2]. The International Roadmap for Devices Systems (ITRS) in 2017 itself defined the 5 nm node which was assumed to be end of Moore's law (scaling by 30% is the Moore magic no.). The quantum tunneling through gate oxide layer following the 7 nm node has provided wings in increasing the chip complexities. IMEC, Cadence and Samsung have already announced the outline for using Gate-all-around technology to produce 3nm chips by 2021. The area and leakage power are very critical in shrinking technology nodes. This paper targets the 6T SRAM cell design and issues faced during the design along with their solutions spread across different technology nodes [3-8].

II. CONVENTIONAL 6T SRAM

The comprehensive basics of 6T SRAM are covered. One can understand SRAM as a latch circuit or flip-flop in which data is stored in bits (data 0 or data 1). This circuit consists of two cross coupled inverters as shown in Fig. 1. CMOS inverter is considered in place of resistive load inverter as it has high noise margin and zero static power dissipation. A 6T SRAM cell is depicted in Fig 1 (c).

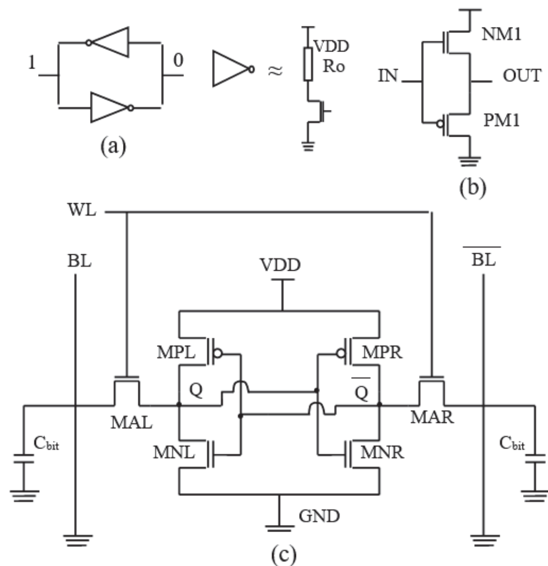

Fig. 1. (a) Cross-coupled Inverter Latch (b) Buffer Circuit (c) Conventional 6-T SRAM Cell

The CMOS implementation of inverter circuit plays real part in storing the data bits. The transistor MPL and MPR forms the PUN and transistors MNL and MNR forms the PDN. PMOS has the holes as the majority carriers while NMOS has the electrons as the majority carrier. The electron mobility is 2.7 times higher than the hole mobility. So, the PMOS should be larger than the NMOS transistors to have equal rise time and fall time of the circuit. This makes the resistance of the transistors equal when sizes of the PMOS transistors are kept approximately 3 time larger as compared to the NMOS transistors. Due to this the SRAM cell face the size issues.

III. CELL OPERATION

SRAM cells have three modes of operation namely i) standby mode (also called as standby mode), ii) read mode, iii) write mode. In hold mode the 'Word Line' (WL) is set to a low-voltage level. Due to this a logic '0' is applied to the access transistors MAL and MAR. This secludes the 'Bit Line' (BL) and 'Bit Bar Line' (BLBAR) from the internal nodes.

ISSN 2305-7254

In the read mode both the BL and BLBAR signals lines are pre-charged to a high-voltage level before turning on the cell. Because of charge on BL, the charge on the internal nodes will get disturbed. In case the inverters are not strong (inverters have small SNM) then bit lines may not get discharged to the desired value [1].

A. Read Operation

For read operation 'Word Line' (WL) is activated to high-voltage level. If the read is done just after the write operation the BL and BLBAR get pre-charged to a high voltage level. As soon as the WL gets activated both access transistor (MAL and MAR) are enabled which establish a connection between the internal nodes and the BL and BLBAR signal lines. If the storage node is initially at logic '1' i.e. Q=1 then MPR, MNL will be OFF and MNR, MPL will be ON, as depicted in Fig. 2. The internal node Q and BL are at same logic '1' potential due to which no potential drop takes place through MAL by the 'Bit Capacitance' (Cbit). Hence MAL will be in cutoff and MAR is in saturation region [1].

Also, the internal node QBAR is at logic '0' and BLBAR is at logic '1'. Hence the Cbit discharge through MAR transistor and the voltage of BLBAR starts decreasing. There will be current flow from MAR to MNR as seen from Fig. 2 [9-10]. Let the voltage at some point of time be V1 such that V1 > V_{TH} of MNL then transistor MNL turns ON. This would change the Q logic '1' to '0' and QBAR logic '0' to '1' thereby conflicting the read operation. This must not be happen as shown in Fig. 3. Therefore the (W/L) ratio must be kept such that V1<V_{TH} of MNL while designing for successful read operation. The BLBAR decrease by 100mV at each pulse, but BL remains constant [11-13]. During read operation data integrity must be maintained to avoid any data loss. The condition for Read Stability can be illustrated as follows:

$$\text{Cell Ration} = (W_{access}/L_{access})\,/(W_{pull\ down}/L_{pull\ down}) \qquad (1)$$

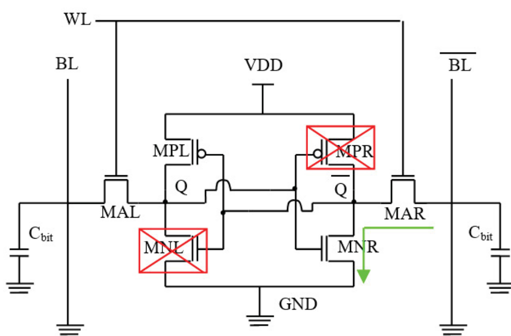

Fig. 2. Read Operation when Q=1 and QBAR=0

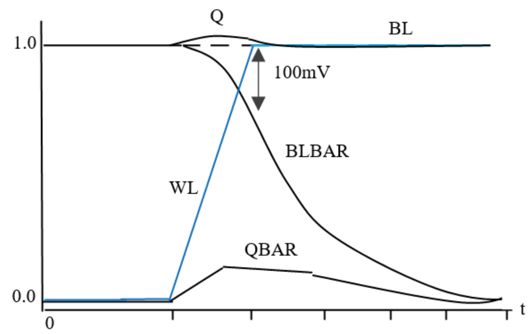

Fig. 3. Read Operation for 6T SRAM cell

B. Write Operation

For write operation, WL is activated to high-voltage level and BL and BLBAR lines are connected to logic '0'. So, during the read operation, both lines act as output lines whereas in case of write both lines act as input lines. Since both lines are low-voltage level and WL is activated, this enables both access transistors [1]. Similarly, for read operation if the storage nodes are initially at logic '1' i.e., Q=1 and QBAR=0 then as evident in Fig. 4 signals QBAR and BLBAR are as same logic level '0'. So, the access transistor MAR turns-off due to which there is no discharge path of capacitance. Also, since Q is at logic level '1' and BL is at logic level '0' which provide a discharging path for C_{bit} through MAL. As signal Q=1, QBAR=0 transistor MNR, MPL turns ON and MPR, MNL turns OFF [9-10]. Let at some point of time, the voltage at Q is VQ, to write the value in SRAM cell the logic at node Q must be changed from logic '0' and QBAR must have logic '1'. For this MNR must be turned OFF and this is only possible when the voltage at Q reduces below the threshold voltage of MNR [11]. When VQ<V_{TH} then the logic gets inverted as MNR turns OFF. Therefore, for easy write operation W/L of pull-up transistor to W/L of access transistor must be small. The write operation is shown in Fig. 5 [12], [13]. The condition for Write Stability can be illustrated as follows

$$\text{Cell Ration} = (W_{Pullup}/L_{Pullup})\,/(W_{access}/L_{access}) \qquad (2)$$

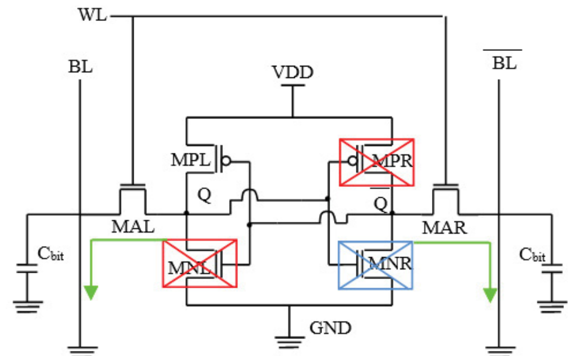

Fig. 4. Write Operation when Q=1 and QBAR=0

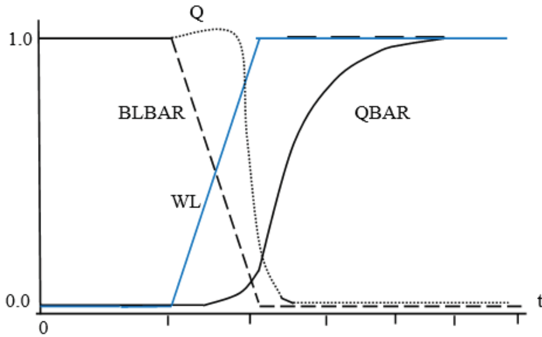

Fig. 5. Write Operation for 6T SRAM cell

IV. DESIGN ISSUES 6T SRAM

The technological advancements in fabrication have enabled the transistor scaling in a very positive manner. But alongside, it has also created new challenges for chip designers. The leakage issues, power densities have severely affected the circuit reliability. Because of these the low leakage SRAM become more critical to design efficiently as approximately 30% of the total chip consumption is because of memory circuits. The today's technology have increased the leakage current to about 86% and decreased the static noise margin by 55% while transferring the technology from 130nm to 32nm [1, 13]. Various issues and challenges that must be faced while designing SRAM are illustrated in this section.

A. Static Noise Margin (SNM)

SNM is a critical parameter for evaluating the stability of the SRAM circuit under static conditions. One can define SNM as the minimum DC noise voltage that would be able to flip or change the state of the cell. It can also be defined as the maximum value of DC disturbance/noise that can be easily tolerated by SRAM cell. Graphically it can be measured as the largest size-box that can be drawn in SRAM transfer function (curves of the two inverters to achieve butterfly curve) [11]. The SRAM parameters get affected by PVT variations easily. SNM depends on pull-up ratio, supply voltage and cell ratio. Static noise margin effects both read and write margin and they correspond to threshold voltages of PMOS and NMOS transistors. However, threshold can be increased to a limit to address such issues. This limitation is because MOS devices generally operate with high threshold value, which are difficult to operate as changing the logic is difficult with higher threshold [14, 29]. By Changing the 'Cell Ratio' (CR) the variation in speed of SRAM can be controlled. With increase in CR, the size of transistors also increases due to which the current flow increases, hence speed also get enhanced. The VTC of the two cross coupled inverters is shown in Fig. 6 (b). This is called as "Butterfly Curve" but there is limitation that butterfly curve does not have automatic in-line testers for measuring SINM (Static Current Noise Margin) [15]. Unexpected flipping of cell can cause instability of the SRAM cell [13]. There are several parameters on which SNM is hinging. These include factors such as temperature, supply voltage and doping variations or sizing in the cell [16]. SNM can be analyzed as Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM) as discussed further in the section.

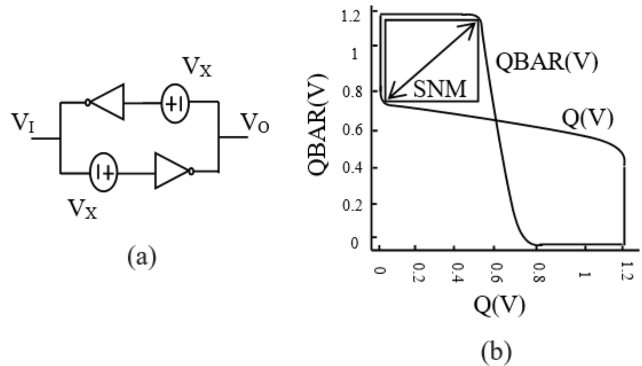

Fig 6. (a) SNM Circuit (b) SNM Butterfly curve

1) Read Static Noise Margin (RSNM)

If the cell structure is not properly designed, then the state can be altered during the read and write operations. Read SNM is calculated when word-line is set to logic '1' and both BL and BLBAR are pre-charged to logic '1'. The storage node of the memory representing '0' state gets pulled upward by the access transistor because of voltage driving effects. This extension in voltage, severely demeans the SNM during the read operation of SRAM. During read operation the stored logic '0' can be changed to logic '1' only when the voltage of node containing logic '0' reaches the V_{TH} of NMOS to pull down the node containing logic '1' to logic '0'. It also happens due to the feedback mechanism for the node containing logic '0'which is pulled up even more far to logic '1'. This results in incorrect data being read or a destructive read as shown in Fig. 7 [17-19].

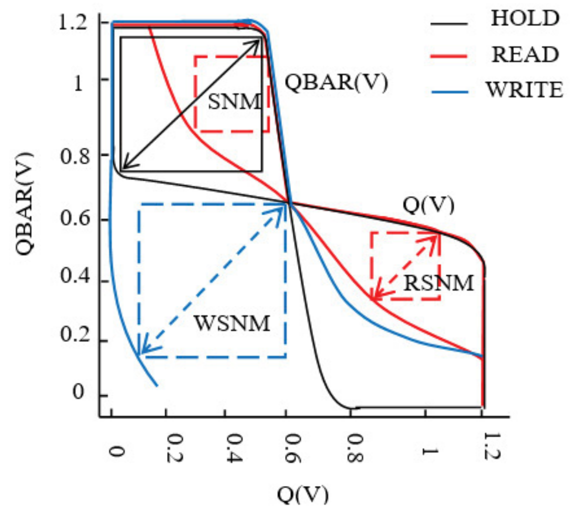

Fig. 7. SNM Characteristics during standby, read and write operation

2) Write Static Noise Margin (WSNM)

WSNM is the least, bit line voltage required to flip the state of the cell. It is the ability by which data can be written in the memory or SRAM cell. When the noise exceeds the write margin voltage (WMV) then the problem occurs i.e., write operation gets failure [17]. WMV is nothing but the maximum noise voltage present on the bit lines during a successful write operation. During writing logic '1' operation in SRAM the write operation performs. So, threshold voltage exceeds the voltage of NMOS transistor for writing '1' and it decreases for writing logic '0'. For successful writing logic '1', only one cross point is to be found on the butterfly curve which states that the cell is in mono-stable state [18]. WSNM for writing logic '1' is the width of the small square that can be encapsulated between the lower right half of the curves. Therefore, if a cell has lower WSNM it means it has poor write ability. The characteristics are shown in Fig. 7 [17-19], [30].

3) Optimization methodologies for SNM

Some solutions are given to tackle the static noise margin (SNM) problem in SRAM for the different technology nodes as listed in Table I.

TABLE I. SNM SOLUTIONS WRT TECHNOLOGY NODES

45nm Technology	65nm Technology
Without increasing transistor count	9T cell
Decreasing WL voltage	11T cell
Increasing BL voltage	8T cell
7T cell	

(a) Without increase in transistor count

In this method the affecting parameters on SNM are changed such that it does not increase the transistor count thereby avoiding area overhead problems. The cell ratio must be 2.5 and pull-up ratio must be 1 so that RSNM of 161mV can be achieved. Also, the voltage should be limited to 50% as power supply reduction beyond that will decrease the RSNM which is not suitable, and the temperature should be kept between 25°C to 50°C.

(b) Decreasing Word-Line Voltage

The stability in SRAM can also be increased by reducing the maximum, word-line voltage to maintain read operation. As the word line voltage approaches to 0, SNM will approach to its be maximum. By reducing word line voltage to minimum or reducing 1V can increase the RSNM by approximately 60% [17].

(c) Increase Bit-Line Voltage

The stability in SRAM can also be increased by increasing the maximum bit line voltage to maintain read operation. As the bit line voltage increases, the SNM will also be increased. On increasing bit line voltage by 50% the SNM can be increased by approximately 33% [17].

(d) 7T SRAM Cell

Fig. 8 shows the 7T SRAM having independent reading and the writing sections which do not interfere with each other mutually. The NMOS transistor MNL2 and MNR2 forms a latch and used to store the data whereas MNL2 and MNR2 and MNM are read access transistors and the PMOS transistors MPL and MPR are for write access. During read operation there is no disturbance in the storage node. The power dissipation of this cell is almost negligible and read margin & write margin are around 1-2mV. Read and write delays are 0.2nS with coverage area around 0.4μm^2. The overall performance is better [20].

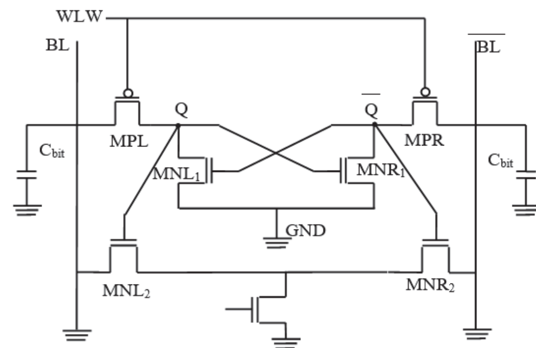

Fig. 8. 7T SRAM cell

(E) 8T SRAM Cell

As depicted in Fig. 9, the modified 8T SRAM cell formed by the write access transistor namely MAL which is controlled by the signal WLW and the read transistor namely MNRM which is controlled by the WLR. During the write operation the logic '1' is applied to WLW with WLR and BLBAR maintained at logic '0' or ground. The MNRM will be in cut off region. To write logic '1' in the cell the BL is pre-charged to VDD. This value is forced to the MAL therefore only single bit line can perform write operation. During the read mode, the WLR is at logic '1' while maintaining WLW to the ground. In this case MAL will be in cut off region. BL and BLBAR are pre-charged to high logic level. If Q=1 and QBAR=0 then BL will get discharged through MNOT and MNRM. Since MAR is in cutoff region there is no discharge of BLBAR so it will be at high logic level. By this method the stability is increased by 80%

Using the 9T the RSNM and WSNM can be increased by approximately two times and with 23% less leakage than conventional SRAM by using super cutoff method. SNR can be increased up to six times by using 11T but in that case area overhead maybe increased by 22 to 28%. Other topologies can solve these issues [21], [22].

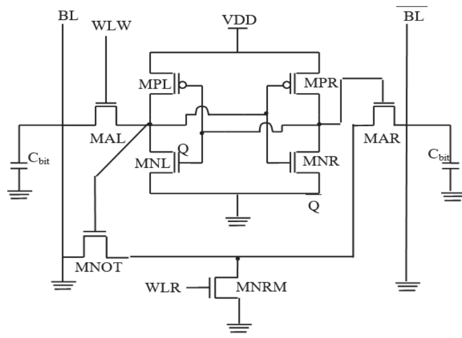

Fig. 9. Modified 8T SRAM cell

B. Leakage Power

Leakage power is very critical factor as the number of mobile users and other battery-operated devices are increasing at a rapid rate. It can be a problem because of noise and heat that is generated due to high density SRAM. Reducing power is censorious as it accounts for less power dissipation i.e. active time of circuit will be less. It is important to maintain reliability in the circuit [23].

Power leakage leads to rise in temperature of the SRAM cell and hence the system as well. The temperature rise affects the device in both states while when it is ON and when it is OFF. In the ON state the cell will be affected by threshold voltage (V_{TH}) and the mobility (μ) of the charged carriers which reduces as temperature rises and lead to change in drain current (ID). In the OFF state the cell is affected by the number of intrinsic carrier (Ni) which increases with temperature. Temperature does not affect majority carrier that much, so the device is more intrinsic. Hence as the temperature rises the leakage current also rises which again increase the temperature. This becomes a vicious cycle which may breakdown the device. To avoid such happening the on-chip temperature must be maintained [24]. There are three sources responsible for power dissipation as mentioned subsequently. The total power dissipation is

$$P_T = P_S + P_D + P_{SC} \quad (3)$$

1) Static Leakage Power (PS)

Consider Fig. 1(b) replace the position of NMOS and PMOS transistor than it will act as CMOS inverter i.e. when the input is logic ‘0’ then the output will be logic ‘1’ and when the input is logic ‘1’ then the output will be logic ‘0’. In this case one transistor always remains off. So, there is no direct path from VDD to GND and the output has steady state current. Hence the static power is zero in this case. However due to reverse bias leakage between the substrate and the diffusion region there is some small amount of static dissipation along with this there is sub-threshold current. The static power is given by:

$$P_S = i_{leakage} * VDD \quad (4)$$

$$P_S=(I_{Sub\text{-}Th} + I_{gate} + I_{contention} + I_{junction})*VDD \quad (5)$$

It also occurs due to junction leakage between source and drain along with gate leakage i.e., from gate and contention current in various circuits [29]. It is shown in Fig. 10.

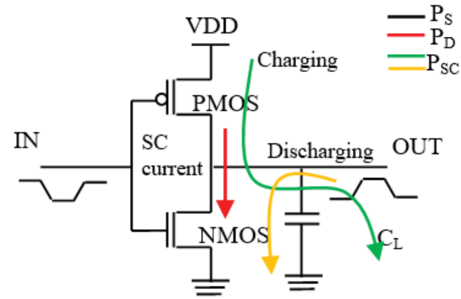

Fig. 10. Leakage Power in SRAM

2) Dynamic Leakage Power (PD)

The switching between load capacitance and short circuit current when transistors are ON is the main cause of dynamic power dissipation. During switching from logic ‘0’ to logic ‘1’ or from logic ‘1’ to logic ‘0’ there is a short period of time when both NMOS and PMOS are turned ON due to this short current pulse will flow from VDD to GND which is required in charging and discharging of the capacitor or capacitive load across output. This results in short circuit dissipation which rest on input rise time and fall time of the design. If the input is repetitive step, then the dynamic power dissipation will depend on energy that is needed for charging and discharging of capacitor [24], [25].

$$P_D = C_L VDD^2 F_P \quad (6)$$

$$PD = P_{switching} + P_{short\text{-}circuit} \quad (7)$$

The dynamic power dissipation can be maintained by both reducing capacitive load, clock frequency and the supply voltage. Some advance methods are also there such as pipelining and reducing switching activity which will reduce the dynamic power up to a great extent as shown in Fig. 10.

3) Short Circuit Leakage Power (P_{SC})

It is due to direct current-path between the supply voltage and the ground. There is time when both NMOS and PMOS are switched ON. This mainly depends on rise time and fall time of the device are quite large and on load capacitance when it is small. This can be reduced by decreasing W/L ratio, supply voltage and capacitance which can be achieved by scaling. The short circuit power dissipation is only in case of static logic gates not in dynamic logic gates because in them there is no path of current and the transistors never get simultaneously ON. It can also be reduced by decreasing transition time at the input [24], [25].

$$P_{short\text{-}circuit} = K.(VDD - 2V_{TH})^3 \tau.N.f \quad (8)$$

4) Optimization of Leakage Power

Some solutions are given to tackle the power dissipation problem in SRAM for the different technology nodes as listed in Table II.

TABLE II. LEAKAGE POWER SOLUTIONS WRT TECHNOLOGY NODES

32 and 45nm Technology	Revamp 8T SRAM Cell
65nm Technology	Recast 6T SRAM Cell
90nm Technology	5T SRAM Cell
180nm Technology	8T SRAM with Sleep Transistors

(a) Revamp 8T SRAM Cell

In this design there are in total five NMOS transistors and three PMOS transistors. The two extra transistors that are added on the path of VDD are used to provide different voltage levels. In the active mode the inverter is connected to VDD through P whereas in the idle mode the voltage supplied is less than the VDD through the N transistor thus to reduce the power scaling dynamic voltage scaling technique is used. To obtain low power operation the access transistors and the pass transistors are supplied by high threshold voltage. This has almost negligible power leakage about 99.85% leakage power is reduced [26] shown in Fig. 11.

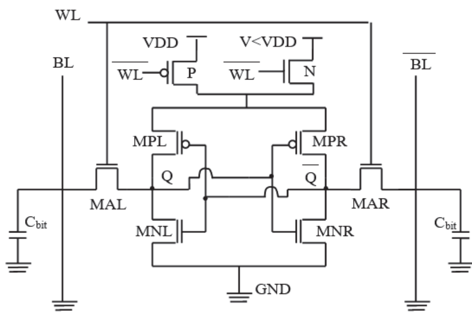

Fig. 11. Revamp 8T SRAM Cell with least leakage power

(b) Recast 6T SRAM Cell

It is an extension of conventional 7T SRAM cell. The advantage of this is that it occupies less area, so the area overhead is lower than 7T. It uses a single transistor for the read operation. In the design shown in Fig. 12, the MNL will always remain in cut off region. This improves the write margin and reduces the acrimony between MAL and MNL. But this degrade the hold margin so to recover MNL is used as low threshold voltage transistor while the MAL is used as higher threshold voltage transistor. WL should be active low. These conditions ensure that hold zero error is removed from the cell. Read errors cannot occur as the BLR cannot disturb the storage node because the trip voltage of the inverter is high. This design has almost 14% less leakage power than the conventional 6T SRAM cell [27].

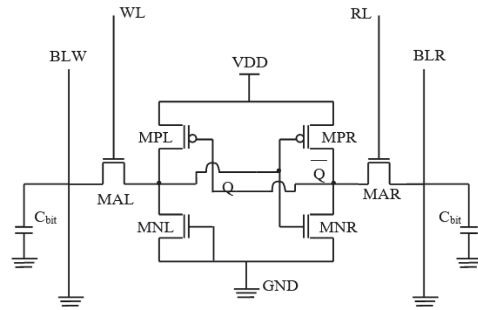

Fig. 12. Recast 6T SRAM Cell with least leakage power

(c) 5T SRAM Cell

In the circuit given in Fig. 13 there is only one access transistor, and the BL is controlled by the pulses. If the storage node (Q) =1, then during the read phase the BL is pre-charged to logic '1' and when the WL is enabled the access transistor is turned ON. The storage node values are transferred to the bit line BL. Write operation can be done by applying BL line with required data value (e.g., for writing '1' apply logic '1') to BL. Through this design 94% leakage power can be reduced also the area is reduced by 30% [28].

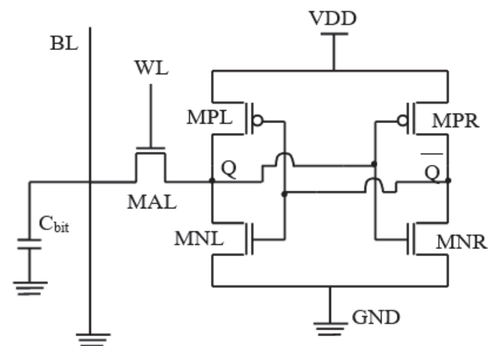

Fig. 13. 5T SRAM cell

(d) 8T/10T SRAM with Sleep Transistors

As shown in Fig. 14, a sleep transistor is used to reduce the leakage power in the SRAM cell. Using this 8T SRAM with sleep transistor the power dissipation is reduced by 98.87% and by using 10T SRAM with sleep transistor power dissipation is reduced by 98.11%. [26]. 8T SRAM has two data output transistor that serve as a dual port. Due to separation of data output and retention there is no relation left between cell current and SNM. There is no decrease in cell current and the value of RSNM is 1.22. Cell current can be improved by decreasing the threshold voltage of NMOS transistor, but this would increase the area by 30% approximately as compared to conventional 6T SRAM.

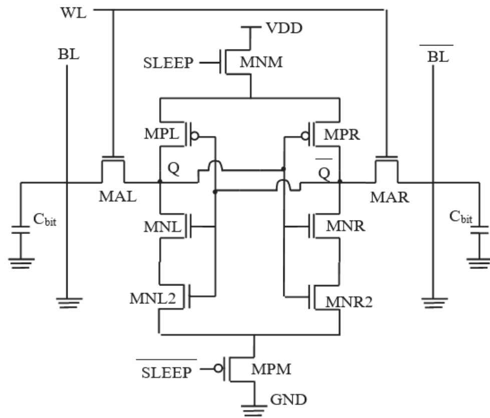

Fig. 14. 8T SRAM with sleep transistors

V. Conclusion

In this paper authors have done comprehensive analysis for the static noise margin and leakage power issues in the conventional 6T SRAM. Different technology nodes are selected for the same. Smaller technology nodes like 22nm 14nm, 7nm 5nm are not considered because of their high production cost involved. Different solutions for the said issues are analyzed. 7T cell provide better SNM with 1μW power as compared to 40μW power for 6T cell. The data integrity is better with well-maintained leakage factor. Better leakage power (94% improvement) reported for 5T with lesser area (30% reduction) as well.

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