Implementing an embedded digital pulse compression filters for primary surveillance radar

Prepared by A. Beseda
NRPL Group

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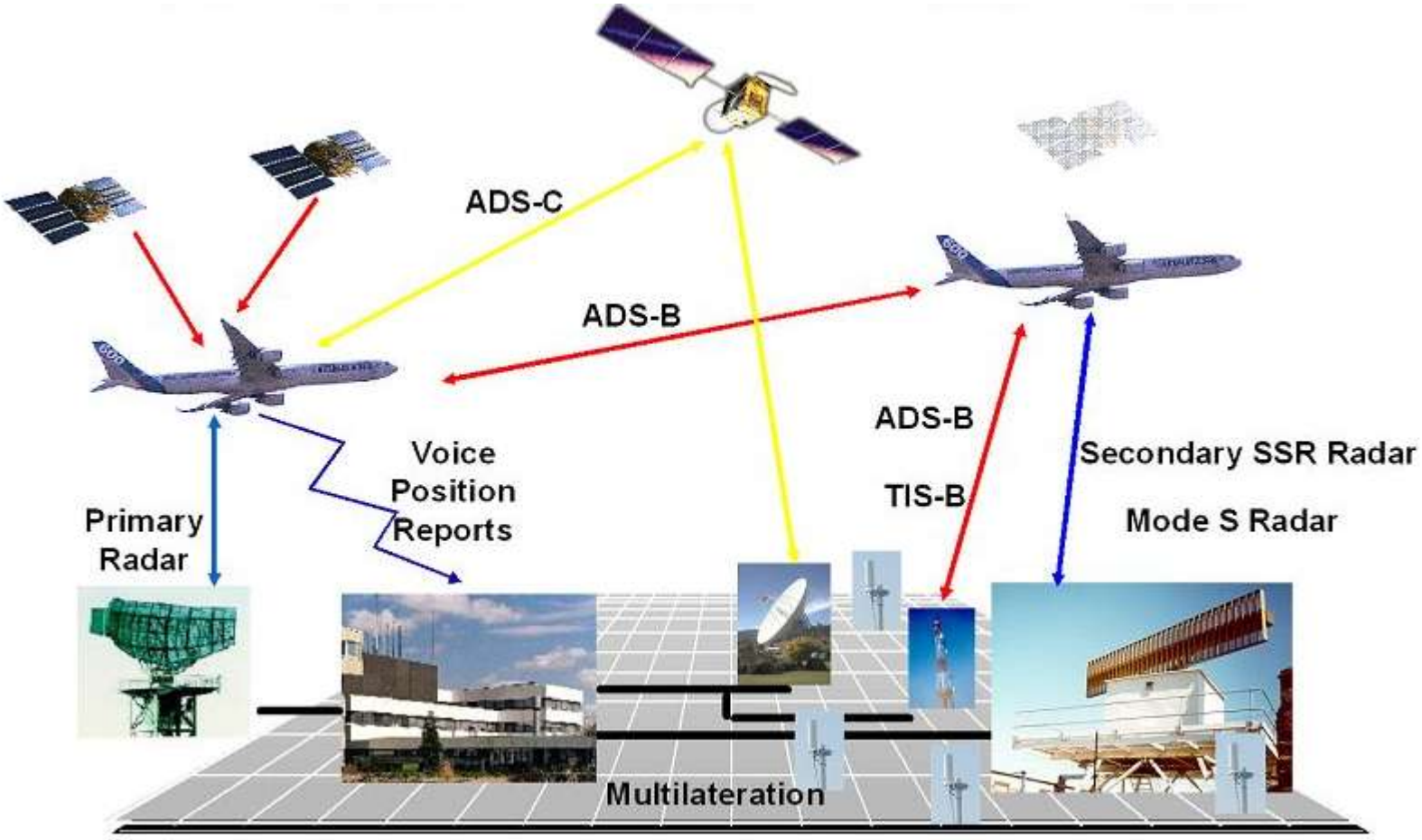
- International Group of Air Traffic Control and IT Systems Companies with headquarters in Vantaa, Finland
- Group Members in Finland, Czech Republic
- More than 400 professionals in development and production

since 1992

Air traffic control system



Primary radar advantages and disadvantages

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Advantages

- Non co-operative
- Many applications
  - Surveillance
  - Surface Movement
  - Weather
  - Civil and military use
- ATC redundancy layer
- Military requirement

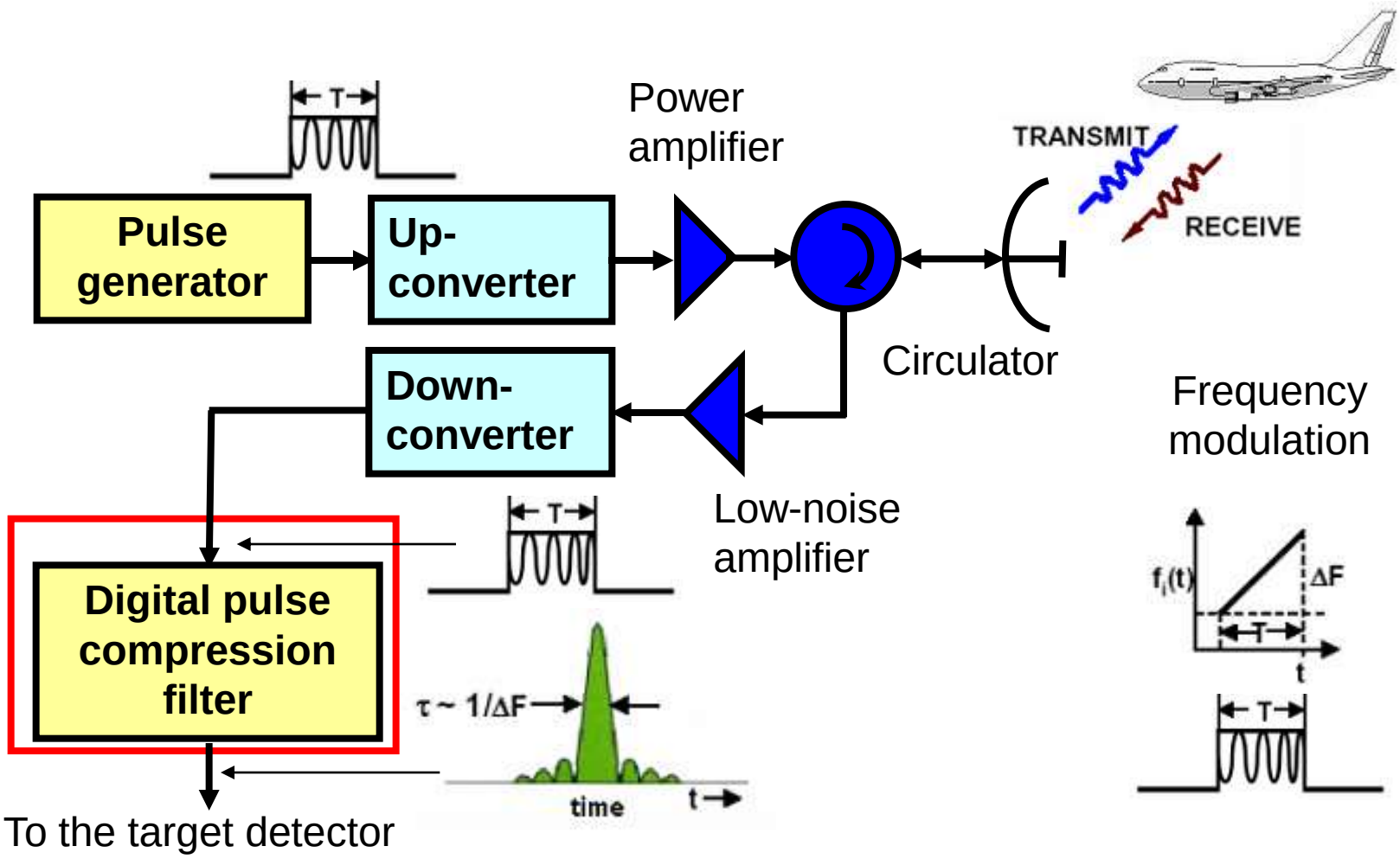
Disadvantages

- Costly
- Complex processing
- No aircraft identity
- False alarms

«Morava» radar station description

- Digital radar signal processing system;
- Coherent receiver and transmitter provide detection quality improvement;
- **Solid-state transmitter with air cooling;**
- Linear and circular polarization decrease the influence of weather clutter;
- **Digital generation and compression of signals;**
- Processing a meteorological information;
- Control and monitoring system (CMS);
- Operation of the radar without continuous staff presence;

Using pulse compression in the PSR



Digital pulse compressors

- Digital pulse-compressors – are digital filters with finite impulse response (FIR-filters). They can be matched or quasi-matched
- Minimal number of taps is:

$$N_{Taps\_min} = F_S T,$$

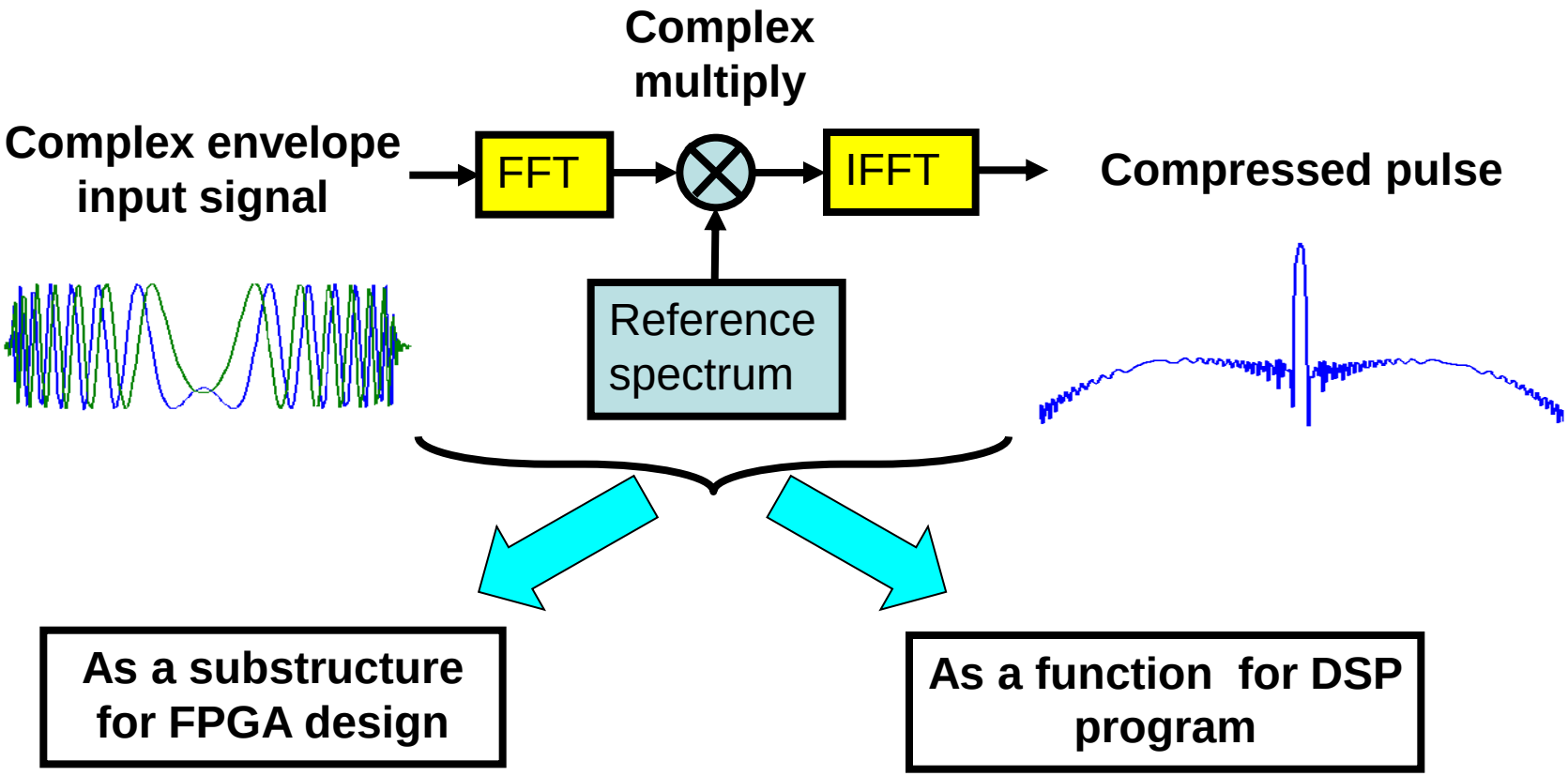
where F_S – sample rate,

T – pulse duration

For airport primary surveillance radars F_S = 2-3 MHz, T= 50 – 100 us, so N_{Taps_min} = 200÷300

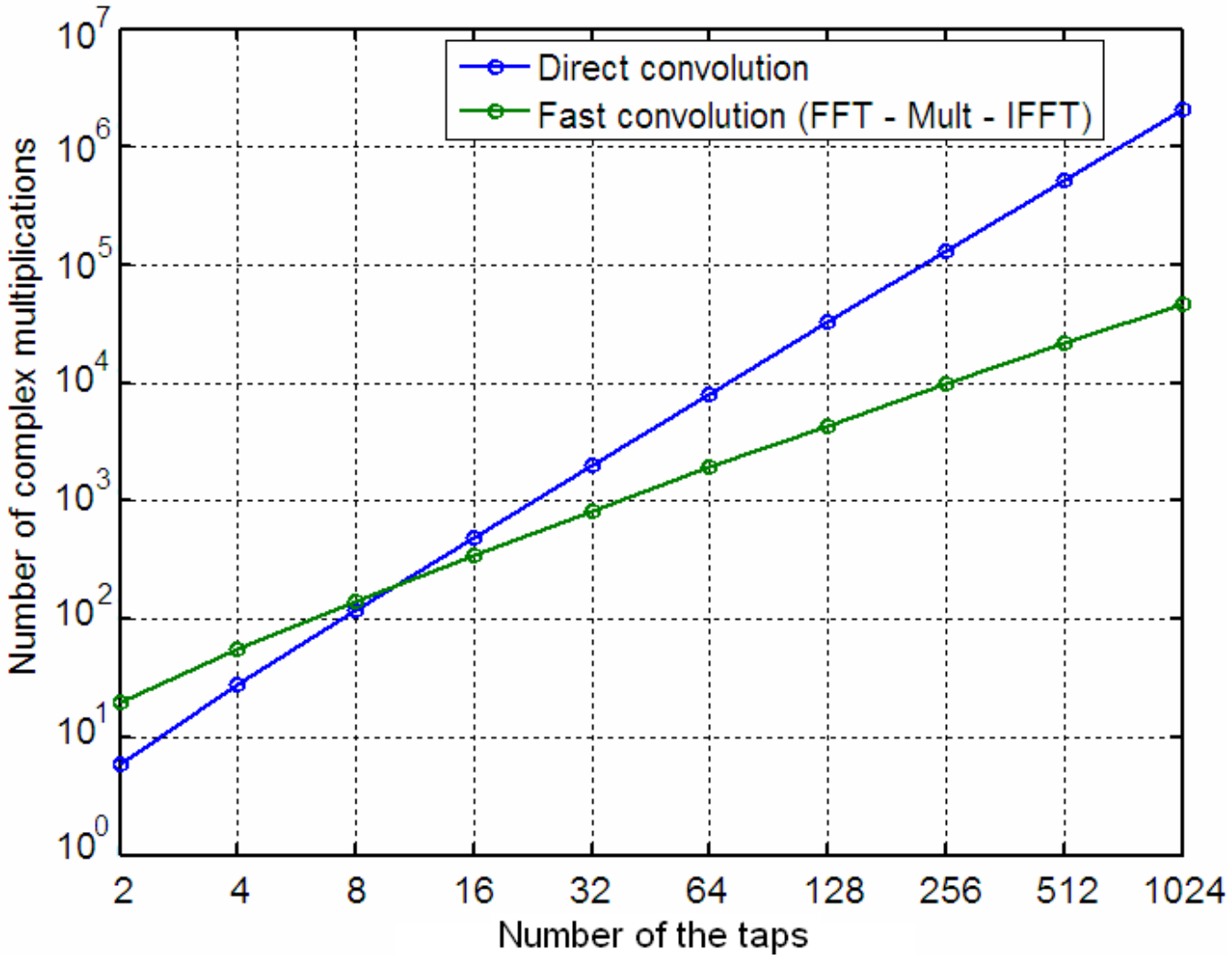
- Number of taps can exceed N_{Taps_min} in several times if Fresnel ripple compensation technique is used
- Pulse compressor necessary embed to signal processor as sub design

Pulse compressors embedding



FPGA – Field-Programmable Gate Array
DSP – Digital Signal Processor

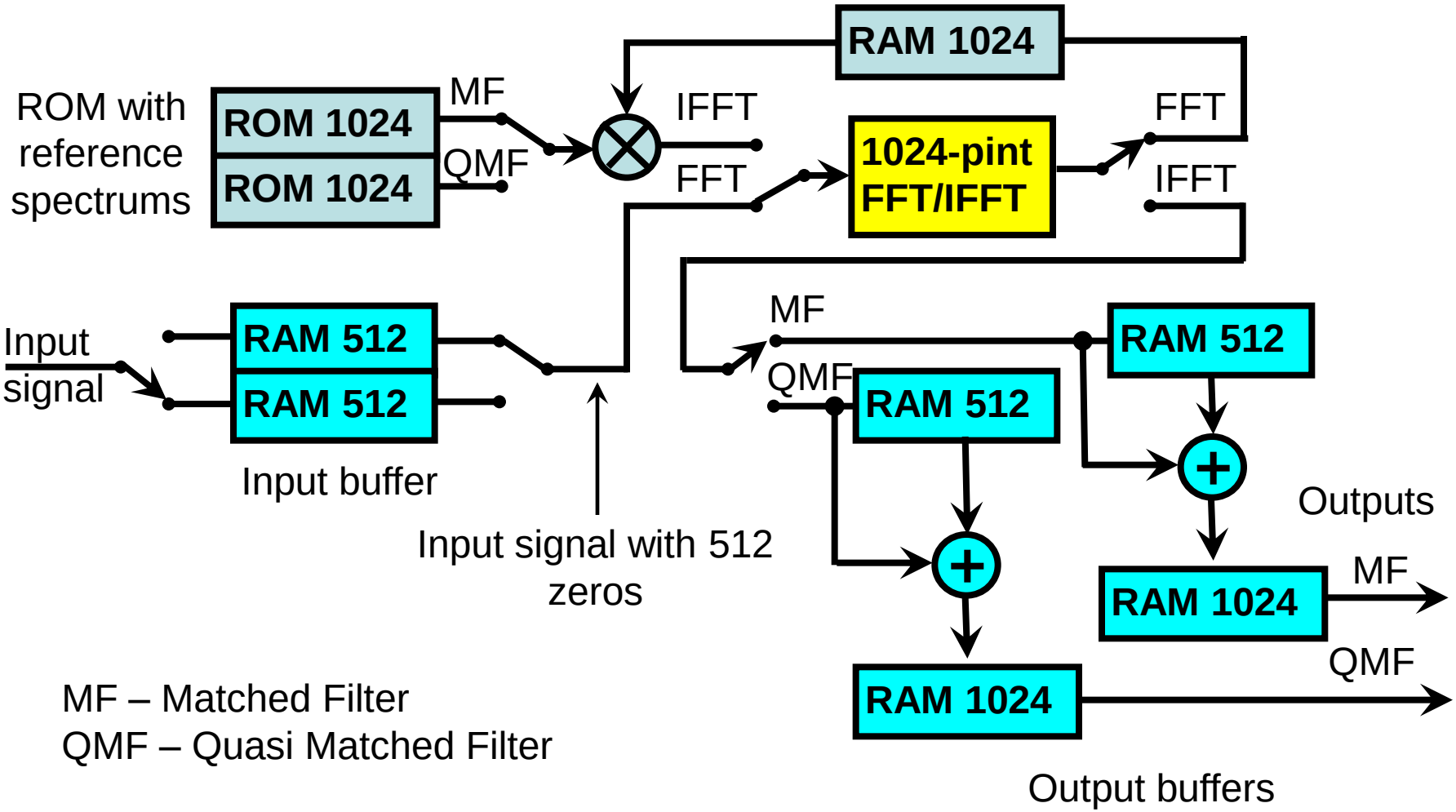
Why fast convolution ?



FPGA pulse compressors

- Advantages
  - High speed
  - Full or partial pipelined processing
  - Flexible source use: space on the chip and/or speed
- Disadvantages
  - Complexity

FPGA stream-continuous dual compressor



MF – Matched Filter
QMF – Quasi Matched Filter

Using Altera FFT IP-core v.2.2.0

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Stratix Device Performance Using the Streaming Data Flow Engine Architecture

Device	Points	Width *(1)*	LEs	18*18 Mults	f_{MAX} (MHz)	Clock Cycle Count	Transform Time (us)
1S20F780C5	2048	16	6,821	18	238.44	2,048	8.58
1S40F780C5	4096	16	7,217	18	230.26	4,096	17.78
1S40F780C5	8192	16	6,973	18	211.82	8,192	38.67

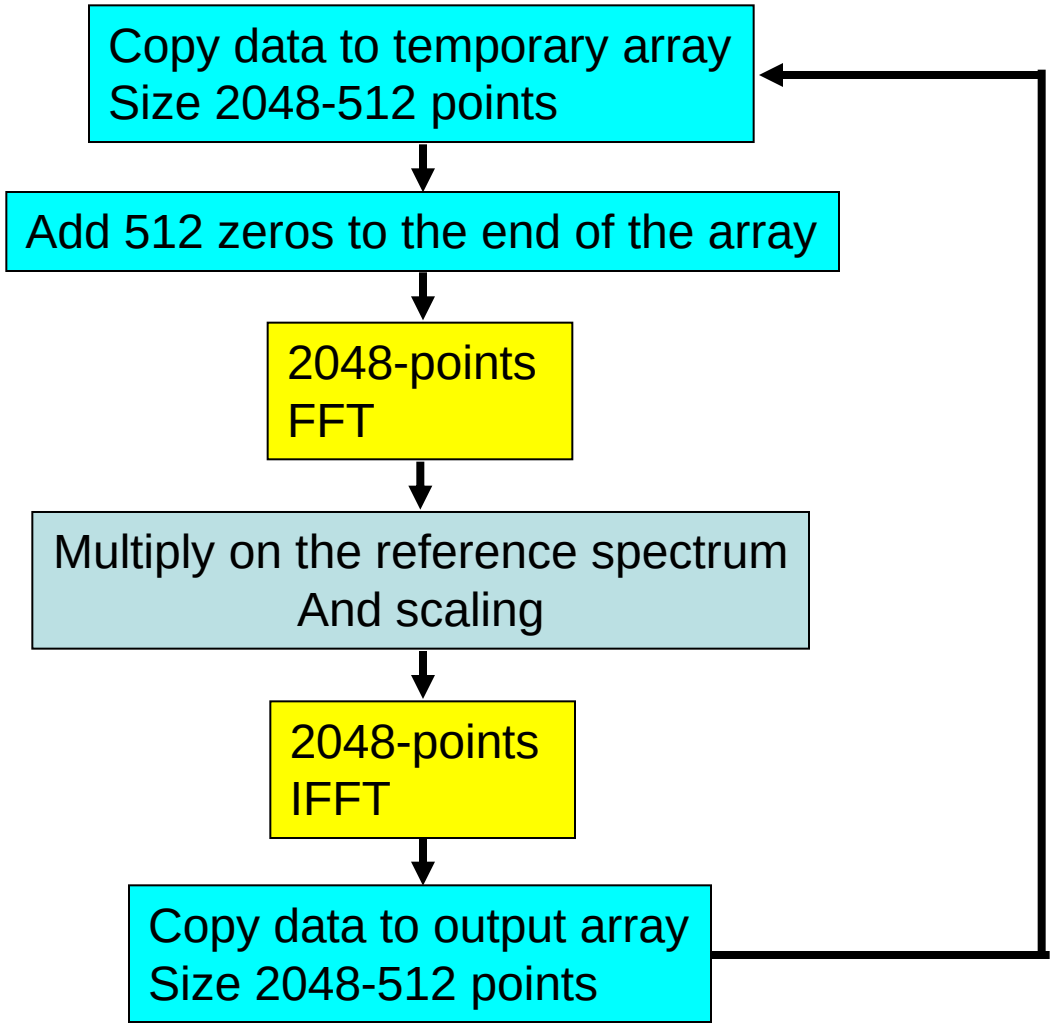
Note
(1) Represents data and twiddle factor precision.

- Radix-4 and mixed Radix-4/2 implementations
- Block floating-point architecture—maintain the maximum dynamic range of data during processing
- Maximum system clock frequency >300 MHz
- Support for multiple single-output and quad-output engines in parallel
- Multiple I/O data flow modes: streaming, buffered burst, and burst
- Transform direction (FFT/IFFT) specifiable on a per-block basis

Digital Compressor as a subprogram for DSP

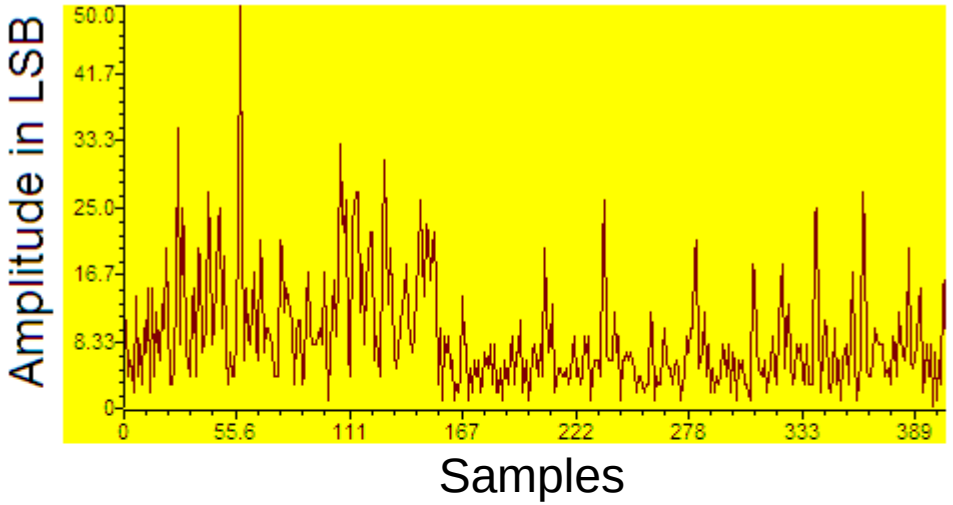
- Advantages
  - Simplicity
- Disadvantages
  - Impossible to increase speed by pipelining inside one processor
  - Fixed point architecture limits dynamic range

Algorithm for DSP for 512-taps compressor

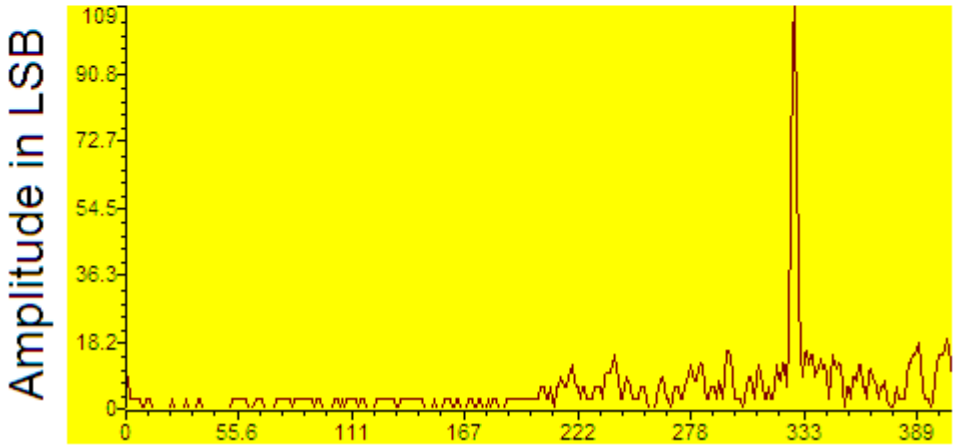


Compression signal in the TMS320C6416T DSP

Envelope of the input signal



Envelope of the output signal



LSB – Least significant bit

Summary

- Primary radars are integral part of the ATC-system
- Pulse-compression technique is used in modern primary radars with solid-state transmitter
- Pulse-compression filters are embedded in the signal processing algorithm
- If FPGA used for data processing high productivity can be achieved

References

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- Rabiner, L. R. and Gold, B., *Theory and Application of Digital Signal Processing*, Prentice-Hall Inc., Englewood Cliffs, NJ, 1975.
- Rodger H. Hosking. *Use FPGA resources to boost radar system performance* http://rfdesign.com/mag/510RFDSF2.pdf
- FFT MegaCore Function User Guide. Version 2.2.0 Altera Corporation