Implementing an embedded digital pulse compression filters for primary surveillance radar

Prepared by A. Beseda
NRPL Group
NRPL Group

- International Group of Air Traffic Control and IT Systems Companies with headquarters in Vantaa, Finland
- Group Members in Finland, Czech Republic
- More than 400 professionals in development and production since 1992
Air traffic control system

- Primary Radar
- Voice Position Reports
- ADS-C
- ADS-B
- Multilateration
- Secondary SSR Radar
- Mode S Radar
- TIS-B
- ADS-B

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Primary radar advantages and disadvantages

Advantages
- Non co-operative
- Many applications
  - Surveillance
  - Surface Movement
  - Weather
  - Civil and military use
- ATC redundancy layer
- Military requirement

Disadvantages
- Costly
- Complex processing
- No aircraft identity
- False alarms
«Morava» radar station description

- Digital radar signal processing system;
- Coherent receiver and transmitter provide detection quality improvement;
- **Solid-state transmitter with air cooling**;
- Linear and circular polarization decrease the influence of weather clutter;
- **Digital generation and compression of signals**;
- Processing a meteorological information;
- Control and monitoring system (CMS);
- Operation of the radar without continuous staff presence;
Using pulse compression in the PSR

- **Pulse generator**
- **Up-converter**
- **Down-converter**
- **Power amplifier**
- **Circulator**
- **Low-noise amplifier**
- **Digital pulse compression filter**
- **To the target detector**
- **Frequency modulation**
- **Transmit and receive**
Digital pulse compressors

- Digital pulse-compressors – are digital filters with finite impulse response (FIR-filters). They can be matched or quasi-matched.

- Minimal number of taps is:
  \[ N_{\text{Taps\_min}} = F_S T, \]

  where \( F_S \) – sample rate,
  \( T \) – pulse duration.

  For airport primary surveillance radars \( F_S = 2-3 \, \text{MHz}, \, T = 50 - 100 \, \text{us} \), so \( N_{\text{Taps\_min}} = 200 \div 300 \)

- Number of taps can exceed \( N_{\text{Taps\_min}} \) in several times if Fresnel ripple compensation technique is used.

- Pulse compressor necessary embed to signal processor as sub design.
Pulse compressors embedding

Complex envelope
input signal

FFT

Complex multiply

IFFT

Reference spectrum

Compressed pulse

As a substructure for FPGA design

As a function for DSP program

FPGA – Field-Programmable Gate Array
DSP – Digital Signal Processor
Why fast convolution?
FPGA pulse compressors

• Advantages
  – High speed
  – Full or partial pipelined processing
  – Flexible source use: space on the chip and/or speed

• Disadvantages
  – Complexity
FPGA stream-continuous dual compressor

Input signal

ROM with reference spectrums

ROM 1024

ROM 1024

RAM 512

RAM 512

Input buffer

Input signal with 512 zeros

MF – Matched Filter

QMF – Quasi Matched Filter

Outputs

RAM 512

RAM 1024

RAM 512

RAM 512

RAM 1024

RAM 1024

RM 1024

1024-pint FFT/IFFT

FFT

IFFT

IFFT

FFT
Using Altera FFT IP-core v.2.2.0

Stratix Device Performance Using the Streaming Data Flow Engine Architecture

<table>
<thead>
<tr>
<th>Device</th>
<th>Points</th>
<th>Width(1)</th>
<th>LEs</th>
<th>18*18 Mults</th>
<th>f_max</th>
<th>Clock Cycle Count</th>
<th>Transform Time (us)</th>
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<tbody>
<tr>
<td>1S20F780C5</td>
<td>2048</td>
<td>16</td>
<td>6,821</td>
<td>18</td>
<td>238.44</td>
<td>2,048</td>
<td>8.58</td>
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<tr>
<td>1S40F780C5</td>
<td>4096</td>
<td>16</td>
<td>7,217</td>
<td>18</td>
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<td>4,096</td>
<td>17.78</td>
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<tr>
<td>1S40F780C5</td>
<td>8192</td>
<td>16</td>
<td>6,973</td>
<td>18</td>
<td>211.82</td>
<td>8,192</td>
<td>38.67</td>
</tr>
</tbody>
</table>

Note
(1) Represents data and twiddle factor precision.

- Radix-4 and mixed Radix-4/2 implementations
- Block floating-point architecture—maintain the maximum dynamic range of data during processing
- Maximum system clock frequency >300 MHz
- Support for multiple single-output and quad-output engines in parallel
- Multiple I/O data flow modes: streaming, buffered burst, and burst
- Transform direction (FFT/IFFT) specifiable on a per-block basis
Digital Compressor as a subprogram for DSP

• Advantages
  – Simplicity

• Disadvantages
  – Impossible to increase speed by pipelining inside one processor
  – Fixed point architecture limits dynamic range
Algorithm for DSP for 512-taps compressor

Copy data to temporary array
Size 2048-512 points

Add 512 zeros to the end of the array

2048-points FFT

Multiply on the reference spectrum
And scaling

2048-points IFFT

Copy data to output array
Size 2048-512 points
Compression signal in the TMS320C6416T DSP

Envelope of the input signal

Envelope of the output signal

LSB – Least significant bit
Summary

• Primary radars are integral part of the ATC-system
• Pulse-compression technique is used in modern primary radars with solid-state transmitter
• Pulse-compression filters are embedded in the signal processing algorithm
• If FPGA used for data processing high productivity can be achieved
References

• IANS Training Programme, 2007
• Rodger H. Hosking. *Use FPGA resources to boost radar system performance*  
• FFT MegaCore Function User Guide. Version 2.2.0 Altera Corporation